L Number	Hits	Search Text	DB	Time stamp
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_	1	("20020016875").PN.	USPAT; US-PGPUB	2004/04/29 17:28
-	33	(710/43).CCLS.	USPAT; US-PGPUB	2004/04/29 17:36
 -	16	3996561.URPN.	USPAT	2004/04/29
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-	10	4959775.URPN.	USPAT	2004/04/29 17:40
-	4	("4494192" "4583160" "4602327" "4630193").PN.	USPAT	2004/04/29 17:41
-	19	(710/122).CCLS.	USPAT; US-PGPUB	2004/04/29 17:45
-	3	5546545.URPN.	USPAT	2004/04/29 17:44
-	7	("4887084" "4914574" "5095460" "5222218" "5274785" "5321640" "5388249").PN.	USPAT	2004/04/29 17:45
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-	966400	daisychain\$7 or (daisy adj chain\$7) or daisy-chain\$7 or cascad\$7 or chain\$7	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2004/04/29 17:48
-	453	((710/8-19).CCLS.) and (daisychain\$7 or (daisy adj chain\$7) or daisy-chain\$7 or cascad\$7 or chain\$7)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2004/04/29 18:12
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-	8	5564114.URPN.	USPAT	2004/04/29 17:59
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-	17	5539390.URPN.	USPAT	2004/04/29 18:05
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Dimitrios Stiliadis, Anujan Varma

January 1997 ACM Transactions on Modeling and Computer Simulation (TOMACS),

Volume 7 Issue 1

Full text available: pdf(925.18 KB) Additional Information: full citation, references, citings, index terms, review

Keywords: ATM switch scheduling, field-programmable gate array, hardware simulation

2 Towards a shared-memory massively parallel multiprocessor Daniel Litaize, Abdelaziz Mzoughi, Christine Rochange, Pascal Sainrat April 1992 ACM SIGARCH Computer Architecture News, Proceedings of the 19th annual international symposium on Computer architecture, Volume 20 Issue 2

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A set of ultra high throughput (more than one Gigabits per second) serial links used as processor-memory network can lead to the starting up of a shared-memory massively parallel multiprocessor. The bandwidth of the network is far beyond values found in present shared-memory multiprocessor networks. To feed this network the memory must be serially multiported. Such a multiprocessor can actually be build with current technologies. This paper analyzes the characteristics of such a ...

³ A generic architecture for on-chip packet-switched interconnections

Pierre Guerrier, Alain Greiner

January 2000 Proceedings of the conference on Design, automation and test in Europe

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1 A reconfigurable hardware approach to network simulation

Dimitrios Stiliadis, Anujan Varma

January 1997 ACM Transactions on Modeling and Computer Simulation (TOMACS), Volume 7 Issue 1

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² Practitioners report: Five years of framework building: lessons learned Kurt Madsen

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When developing large software systems, it is often difficult to foresee exactly which tradeoffs are important, and which quality parameters will be of importance down the road. This paper reports experiences from a project in which a large application framework for B2B integration has been continuously developed and used over a five-year period. The framework has been the foundation for a variety of different concrete applications. Here we will report on our experiences from this endeavor.

Keywords: C++, application frameworks, architecture, enterprise application integration, object-oriented programming

The Honeywell Modular Microprogram Machine: M3

E. Douglas Jensen, Richard Y. Kain

March 1977 ACM SIGARCH Computer Architecture News, Proceedings of the 4th annual symposium on Computer architecture, Volume 5 Issue 7

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M3 is intended for research into unconventional special purpose stored program elements of computer systems (for example, a distributed computer Bus Interface Unit). The principal requirements for such a machine are flexibility and modularity. M3 consists of an



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1 <u>Digital talking books on a PC</u>: a usability evaluation of the prototype DAISY playback software

Sarah Morley

January 1998 Proceedings of the third international ACM conference on Assistive technologies

Full text available: txt(38.78 KB)

Additional Information: full citation, references, citings, index terms

Keywords: auditory navigation, blind and visually impaired readers, digital talking books, evaluation methodology, structured information access

² DAISY: dynamic compilation for 100% architectural compatibility

Kemal Ebcioğlu, Erik R. Altman
May 1997 ACM SIGARCH Computer Architecture Nev

May 1997 ACM SIGARCH Computer Architecture News , Proceedings of the 24th annual international symposium on Computer architecture, Volume 25 Issue 2

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Although VLIW architectures offer the advantages of simplicity of design and high issue rates, a major impediment to their use is that they are not compatible with the existing software base. We describe new simple hardware features for a VLIW machine we call **DAISY** (**Dynamically Architected Instruction Set from Yorktown**). **DAISY** is specifically intended to emulate existing architectures, so that all existing softwa ...

 $\textbf{Keywords:} \ \ \textbf{binary translation, dynamic compilation, instruction-level parallelism, object code compatible VLIW, superscalar$

Device selection for system partitioning

Ulrich Weinmann, Oliver Bringmann, Wolfgang Rosenstiel
December 1995 Proceedings of the conference on European design automation

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⁴ Binary translation and architecture convergence issues for IBM system/390

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